L6727

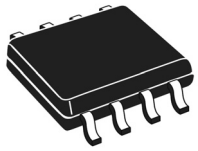
Single phase PWM controller

Feature

- Flexible power supply from 5V to 12V
- Power conversion input as low as 1.5V
- 1% output voltage accuracy
- High-current integrated drivers
- Adjustable output voltage
- 0.8V internal reference
- Simple voltage mode control loop
- Sensorless and programmable OCP across Low-Side R_{dsON}
- Oscillator internally fixed at 300kHz
- Internal Soft-Start
- LS-LESS to manage pre-bias start-up
- Disable function
- OV / UV protection
- FB disconnection protection
- SO-8 package

Applications

- Subsystem power supply (MCH, IOCH, PCI...)
- Memory and termination supply
- CPU & DSP power supply
- Distributed power supply
- General DC / DC converters



SO-8

Description

L6727 is a single-phase step-down controller with integrated high-current drivers that provides complete control logic, protections and reference voltage to realize in an easy and simple way general DC-DC converters by using a compact SO-8 package.

Device flexibility allows managing conversions with power input V_{IN} as low as 1.5V and device supply voltage in the range of 5V to 12V.

L6727 provides simple control loop with voltage-mode error-amplifier. The integrated 0.8V reference allows regulating output voltages with ±1% accuracy over line and temperature variations. Oscillator is internally fixed to 300kHz.

L6727 provides programmable over current protection as well as over and under voltage protection. Current information is monitored across the Low-Side mosfet R_{dsON} saving the use of expensive and space-consuming sense resistors while output voltage is monitored through FB pin.

FB disconnection protection prevents excessive and dangerous output voltages in case of floating FB pin.

Table 1. Device summary

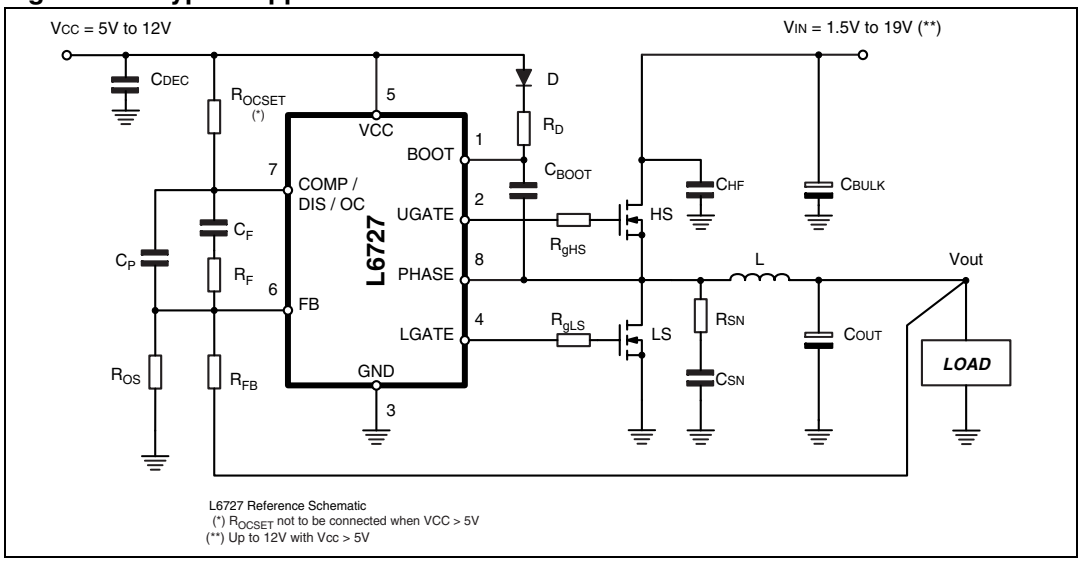
Part Number	Package	Packaging
L6727	SO-8	Tube
L6727TR	SO-8	Tape & Reel

Contents

1 Typical application circuit and block diagram

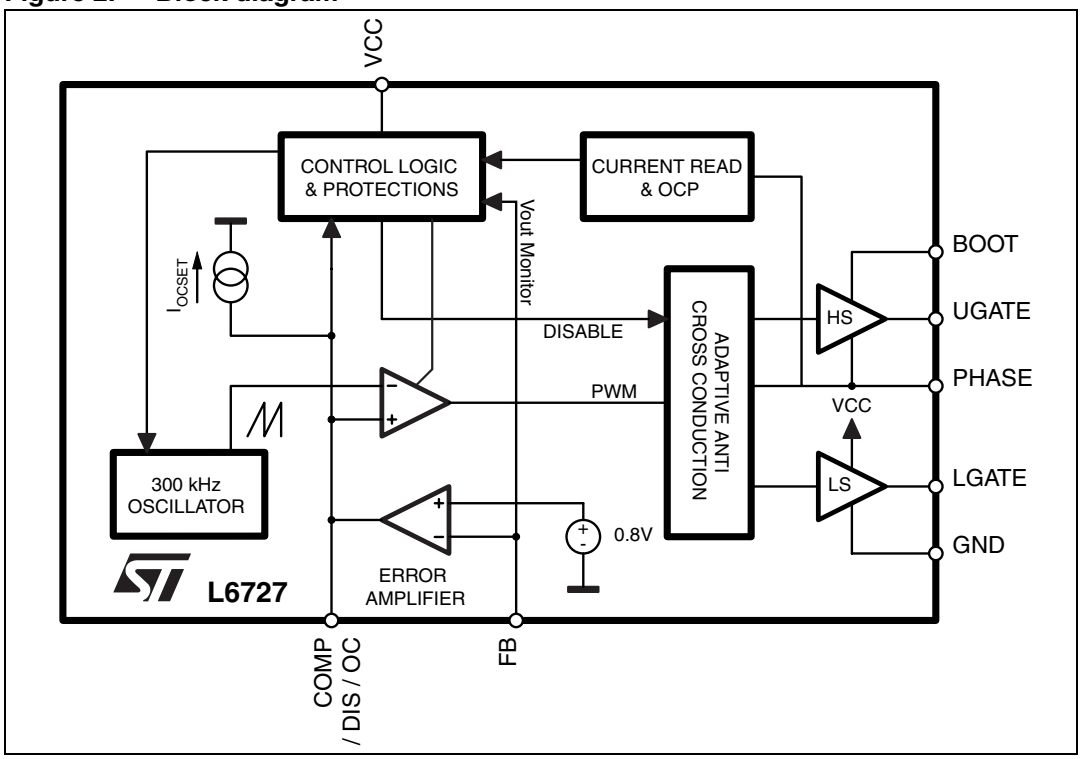
1.1 Application circuit

Figure 1. Typical application circuit



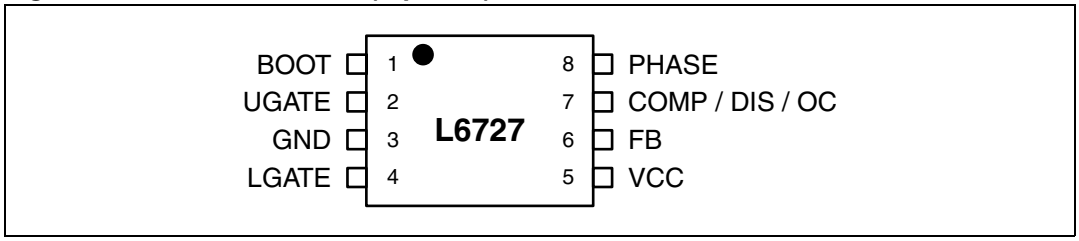
1.2 Block diagram

Figure 2. Block diagram



2 Pins description and connection diagrams

Figure 3. Pins connection (top view)



2.1 Pin descriptions

Table 2. Pins descriptions

Pin #	Name	Function
1	BOOT	HS Driver Supply. Connect through a capacitor (100nF) to the floating node (LS-Drain) pin and provide necessary bootstrap diode from VCC.
2	UGATE	HS Driver Output. Connect to HS mosfet gate.
3	GND	All internal references, logic and drivers are connected to this pin. Connect to the PCB ground plane.
4	LGATE	LS Driver Output. Connect to LS mosfet gate.
5	VCC	Device and LS Driver power supply. Operative range from 4.1V to 13.2V. Filter with at least 1µF MLCC to GND.
6	FB	Error Amplifier Inverting Input. Connect with a resistor R_{FB} to the output regulated voltage. Additional resistor R_{OS} to GND may be used to regulate voltages higher than the reference.
7	COMP / DIS / OC	*COMP.* Error Amplifier Output. Connect with an R_F - C_F // C_P to FB to compensate the control-loop. *DIS.* The device can be disabled by forcing this pin lower than 0.5V(typ). To disable the device, the external pull-down need to overcome 10mA of COMP output current for about 15µs. Once disabled, COMP output current drops to 20µA. *OC.* Over current threshold set. Connect with an R_{OCSET} resistor to VCC (ONLY IF VCC is supplied by 5V bus) to program OC threshold. When VCC > 5V, R_{OCSET} need to be not-connected.
8	PHASE	HS Driver return path, current-reading and adaptive-dead-time monitor. Connect to the LS drain to sense R_{dsON} drop to measure the output current. This pin is also used by the adaptive-dead-time control circuitry to monitor when HS mosfet is OFF.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal Resistance Junction to Ambient(1)	85	°C/W
T_{MAX}	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-40 to 150	°C
T_J	Junction Temperature Range	-20 to 150	°C

1. Measured with the component mounted on a 2S2P board in free air (6.7cm x 6.7cm, 35µm (P) and 17.5µm (S) copper thickness).

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter (1)	Value	Unit
V_{CC}	to GND	-0.3 to 15	V
V_{BOOT}	to PHASE to GND	15 45	V
V_{UGATE}	to PHASE to PHASE; t < 50ns to GND	-0.3 to (V_{BOOT} - V_{PHASE}) + 0.3 -1 V_{BOOT} + 0.3	V
V_{PHASE}	to GND	-8 to 30	V
V_{LGATE}	to GND to GND; t < 50ns	-0.3 to V_{CC} + 0.3 -1	V
	COMP to GND	-0.3 to 7	V
	FB to GND	-0.3 to 3.6	V

1. ESD immunity for FB pin is guaranteed up to ±1000V (Human Body Model).

3.2 Electrical characteristics

Table 5. Electrical characteristics
(V_{CC} = 12V; T_A = -20°C to +85°C, unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Recommended operating conditions						
V_{CC}	Device supply voltage	See *Figure 1*	4.1		13.2	V
V_{IN}	Conversion input voltage				13.2	V
		V_{CC} < 7.0V			19.0	V
Supply current and power-ON						
I_{CC}	VCC supply current	UGATE and LGATE = OPEN		6		mA
I_{BOOT}	BOOT supply current	UGATE = OPEN; PHASE to GND		0.5		mA
UVLO	VCC turn-ON	VCC Rising			4.1	V
	Hysteresis			0.2		V
Oscillator						
F_{SW}	Main oscillator accuracy	0°C to +70°C	270	300	330	kHz
			250	300	350	kHz
ΔV_{OSC}	PWM ramp amplitude			1.5		V
d_{MAX}	Maximum duty cycle		80			%
Reference						
	Output voltage accuracy	V_{OUT} = 0.8V, T_A = 0°C to 70°C	-1	-	1	%
		V_{OUT} = 0.8V	-1.5		1.5	%
Error amplifier						
A_0	DC gain(1)			120		dB
GBWP	Gain-bandwidth product(1)			15		MHz
SR	Slew-rate(1)			8		V/µs
I_{FB}	Input bias current	Sourced from FB		100		nA
DIS	Disable threshold	COMP Falling	0.43	0.5		V

Table 5. Electrical characteristics (continued)
(V_{CC} = 12V; T_A = -20°C to +85°C, unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Gate drivers						
I_{UGATE}	HS source current	BOOT - PHASE = 5V to 12V		1.5		A
R_{UGATE}	HS sink resistance	BOOT - PHASE = 5V to 12V		1.1		Ω
I_{LGATE}	LS source current	VCC = 5V to 12V		1.5		A
R_{LGATE}	LS sink resistance	VCC = 5V to 12V		0.65		Ω
Over-current protection						
I_{OCSET}	OCSET current source	Sunk from COMP pin, before SS	55	60	65	µA
V_{CC_OC}	OC Switch-over threshold	VCC Rising		8		V
V_{OCTH}	Fixed OC threshold	V_{PHASE} to GND, VCC > V_{CC_OC}		-400		mV
Over & under-voltage protections						
OVP	OVP threshold	FB rising		1		V
UVP	UVP threshold	FB falling		0.6		V

1. Guaranteed by design, not subject to test.

4 Device description

L6727 is a single-phase PWM controller with embedded high-current drivers that provides complete control logic and protections to realize in an easy and simple way a general DC-DC step-down converter. Designed to drive N-channel MOSFETs in a synchronous buck topology, with its high level of integration this 8-pin device allows reducing cost and size of the power supply solution.

L6727 is designed to operate from a 5V or 12V supply bus. Thanks to the high precision 0.8V internal reference, the output voltage can be precisely regulated to as low as 0.8V with ±1% accuracy over line and temperature variations (between 0°C and +70°C).
The switching frequency is internally set to 300kHz.

This device provides a simple control loop with a voltage-mode error-amplifier. The error-amplifier features a 15MHz gain-bandwidth product and 8V/µs slew rate, allowing high regulator bandwidth for fast transient response.

To avoid load damages, L6727 provides over current protection as well as over voltage, under voltage and feedback disconnection protection. When the device is supplied from 5V, over current trip threshold is programmable by a simple resistor. Output current is monitored across Low-Side MOSFET R_{dsON}, saving the use of expensive and space-consuming sense resistor. Output voltage and feedback disconnection are monitored through FB pin.

L6727 implements soft-start increasing the internal reference from 0V to 0.8V in 5.1ms (typ) in closed loop regulation. Low-Side-Less feature allows the device to perform soft-start over pre-biased output avoiding high current return through the output inductor and dangerous negative spike at the load side.

5 Driver section

The integrated high-current drivers allow using different types of power MOSFET (also multiple MOSFETs to reduce the equivalent R_{dsON}), maintaining fast switching transition.

The driver for the high-side MOSFET uses BOOT pin for supply and PHASE pin for return. The driver for low-side MOSFET uses the VCC pin for supply and GND pin for return.

The controller embodies an anti-shoot-through and adaptive dead-time control to minimize low side body diode conduction time, maintaining good efficiency while saving the use of Schottky diode:

- to check high-side MOSFET turn off, PHASE pin is sensed. When the voltage at PHASE pin drops down, the low-side MOSFET gate drive is suddenly applied;
- to check low-side MOSFET turn off, LGATE pin is sensed. When the voltage at LGATE has fallen, the high-side MOSFET gate drive is suddenly applied.

If the current flowing in the inductor is negative, voltage on PHASE pin will never drop. To allow the low-side MOSFET to turn-on even in this case, a watchdog controller is enabled: if the source of the high-side MOSFET doesn't drop, the low side MOSFET is switched on so allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

Power conversion input is flexible: 5V, 12V bus or any bus that allows the conversion (See maximum duty cycle limitation and recommended operating conditions, in *Table 5*) can be chosen freely.

5.1 Power dissipation

L6727 embeds high current MOSFET drivers for both high side and low side MOSFETs: it is then important to consider the power that the device is going to dissipate in driving them in order to avoid overcoming the maximum junction operative temperature.

Two main terms contribute in the device power dissipation: bias power and drivers' power.

- Device Bias Power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply quantifiable as follow (assuming to supply HS and LS drivers with the same VCC of the device):

$$P_{DC} = V_{CC} \cdot (I_{CC} + I_{BOOT})$$

- Drivers power is the power needed by the driver to continuously switch on and off the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs (easy calculable) is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term is the important one to be determined to calculate the device power dissipation. The total power dissipated to switch the MOSFETs results:

$$P_{SW} = F_{SW} \cdot [Q_{gHS} \cdot (V_{BOOT} - V_{PHASE}) + Q_{gLS} \cdot V_{CC}]$$

  where V_{BOOT} - V_{PHASE} is the voltage across the bootstrap capacitor.

External gate resistors helps the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.

6 Soft Start and Disable

L6727 implements a soft start to smoothly charge the output filter avoiding high in-rush currents to be required from the input power supply. The device progressively increases the internal reference from 0V to 0.8V in about 5.1ms, in closed loop regulation, gradually charging the output capacitors to the final regulation voltage.

In the event of an over current triggering during soft start, the over current logic will override the soft start sequence and will shut down both the high side and low side gates for the internal soft start residual time (up to 2048 clock cycles) plus 2048 clock cycles, then it will begin a new soft start.

The device begins soft start phase only when VCC power supply is above UVLO threshold and over current threshold setting phase has been completed.

6.1 Low-Side-Less Start up (LSLess)

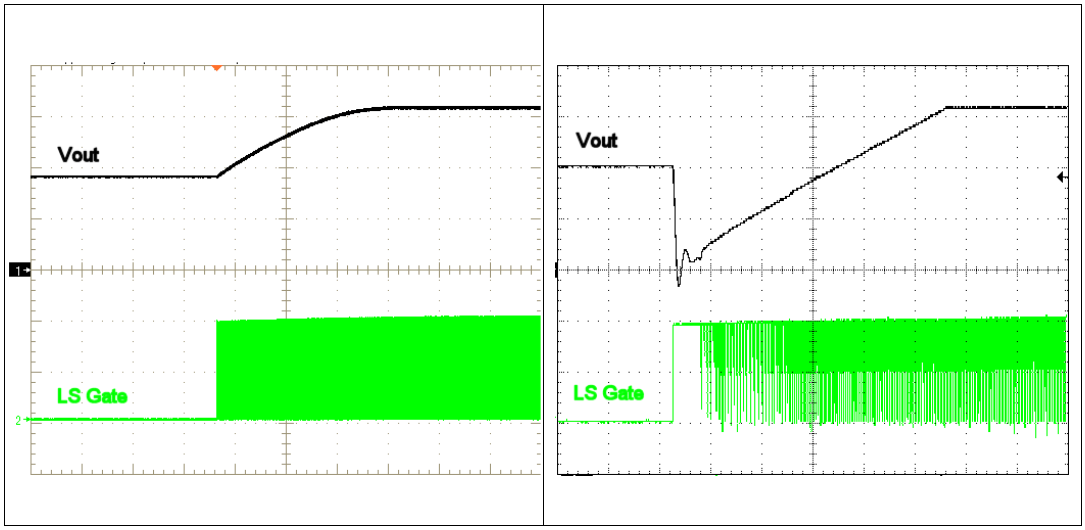
In order to manage start up over pre-biased output, L6727 performs a special sequence in enabling LS driver to switch: during the soft-start phase, LS driver results disabled (LS = OFF) until HS starts to switch. This avoids the dangerous negative spike on the output voltage that can happen if starting over a pre-biased output.

If the output voltage is pre-biased to a voltage lower than the programmed one, neither HS nor LS will turn on until the soft start ramp exceeds the output pre-bias voltage; then V_{OUT} will ramp up from there, without any drop or current return.

If the output voltage is pre-biased to a voltage higher than the programmed one, HS would never start to switch. In this case, at the end of soft start time, LS is enabled and discharges the output to the final regulation value.

This particular feature of the device masks the LS turn-on only from the control loop point of view: protections by-pass LSLESS, turning ON the LS mosfet in case of need.

Figure 4. LSLess Startup (left) vs. Non-LSLess Startup (right)

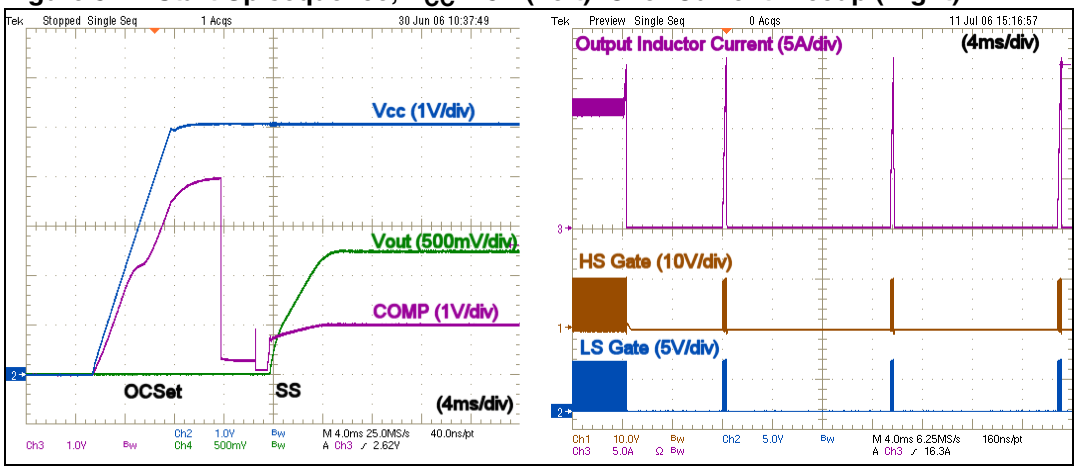


6.2 Enable / Disable

The device can be disabled by externally pushing COMP / DIS pin under 0.5V (typ). In disable condition HS and LS MOSFETs are turned off, and a 20µA current is sourced from COMP / DIS pin. Setting free the pin, this current pulls it over the threshold and the device enables again performing a new SS.

To disable the device, the external pull-down needs to overcome 10mA of COMP output current for about 15µs. Once disabled, COMP output current drops to 20µA.

Figure 5. Start Up sequence; V_{CC} = 5V (Left). Over Current Hiccup (Right)



7 Over current protection

The over current feature protects the converter from a shorted output or overload, by sensing the output current information across the Low Side MOSFET drain-source on-resistance, R_{dsON}. This method reduces cost and enhances converter efficiency by avoiding the use of expensive and space-consuming sense resistors.

The low side R_{dsON} current sense is implemented by comparing the voltage at the PHASE node when LS MOSFET is turned on with the programmed OCP threshold voltage, internally held. If the monitored voltage drop (GND to PHASE) exceeds this threshold, an Over Current Event is detected. If two Over Current Events are detected in two consecutive switching cycles, the protection will be triggered and the device will turn off both LS and HS MOSFETs for 2048 clock cycles (plus internal SS remaining time, if triggered during a SS phase); then it will begin a new Soft Start.

If the over current condition is not removed, the continuous fault will cause L6727 to go into a hiccup mode with a typical period of 13.6ms (*Figure 5*), guaranteeing safe load protection and very low power dissipation.

7.1 Over current threshold setting

When supplied with VCC = 5V, L6727 allows to easily program an Over Current Threshold ranging from 50mV to 500mV, simply by adding a resistor (R_{OCSET}) between COMP and VCC.

During a short period of time (5.5ms - 6.5ms) following the first enable (given VCC over UVLO threshold), an internal 60µA current (I_{OCSET}) is sunk from COMP pin, determining a voltage drop across R_{OCSET}. This voltage drop, differentially sensed between VCC and COMP, divided by a factor 3, will be sampled and internally held by the device as Over Current Threshold until next VCC cycling. Differential sensing versus VCC allows OCSET procedure to be fully independent from VIN rail. The OC setting procedure overall time length ranges from 5.5ms to 6.5ms, proportionally to the threshold being set.

Connecting an R_{OCSET} resistor between COMP and VCC, the programmed threshold will be:

$$I_{OCth} = \frac{1}{3} \cdot \frac{I_{OCSET} \cdot R_{OCSET}}{R_{dsON}}$$

R_{OCSET} values range from 2.5kΩ to 25kΩ.

If the voltage drop across R_{OCSET} is too low, the system will be very sensitive to start-up inrush current and noise. This can result in a continuous OCP triggering and hiccup mode. In this case, consider to increase R_{OCSET} value.

In case R_{OCSET} is not connected (and VCC = 5V), the device will set the maximum threshold.

If the device is supplied with a VCC higher than 7V, R_{OCSET} must be not connected. In this case, as soon as VCC rises over V_{CC_OC} (8V typ.), L6727 switches OC threshold to 400mV (internally fixed value).

See *Figure 5* for OC threshold setting and soft start oscilloscope sample waveforms.

8 Output voltage monitor and protections

L6727 monitors the voltage at FB pin and compares it to internal reference voltage in order to provide Under Voltage and Over Voltage protections.

8.1 Under voltage protection

If the voltage at FB pin drops below UV threshold (0.6V typ), the device turns off both HS and LS MOSFETs, waits for 2048 clock cycles and then performs a new Soft Start. If under voltage condition is not removed, the device enters a hiccup mode with a typical period of 13.6ms.

UVP is active from the end of soft start.

8.2 Over voltage protection

If the voltage at FB pin rises over OV threshold (1V typ), over voltage protection turns off HS MOSFET and turns on LS MOSFET overriding PWM logic as long as over voltage is detected.

OVP is always active with top priority as soon as over current threshold setting phase has been completed.

8.3 Feedback disconnection protection

In order to provide load protection even if FB pin is not connected, a 100nA bias current is always sourced from this pin. If FB pin is not connected, this current will permanently pull up FB over OVP threshold: thus LS will be latched on preventing output voltage from rising out of control.

8.4 Under voltage lock out

In order to avoid anomalous behaviors of the device when the supply voltage is too low to support its internal rails, UVLO is provided: the device will start up when VCC reaches UVLO upper threshold and will shutdown when VCC drops below UVLO lower threshold.

The 4.1V maximum UVLO upper threshold allows L6727 to be supplied from 5V and 12V busses in or-ing diode configuration.

9 Application details

9.1 Output voltage selection

L6727 is capable to precisely regulate an output voltage as low as 0.8V. In fact, the device comes with a fixed 0.8V internal reference that guarantees the output regulated voltage to be within ±1% tolerance over line and temperature variations between 0°C and +70°C (excluding output resistor divider tolerance, when present).

Output voltage higher than 0.8V can be easily achieved by adding a resistor R_{OS} between FB pin and ground. Referring to *Figure 1*, the steady state DC output voltage will be:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{FB}}{R_{OS}}\right)$$

where V_{REF} is 0.8V.

9.2 Compensation network

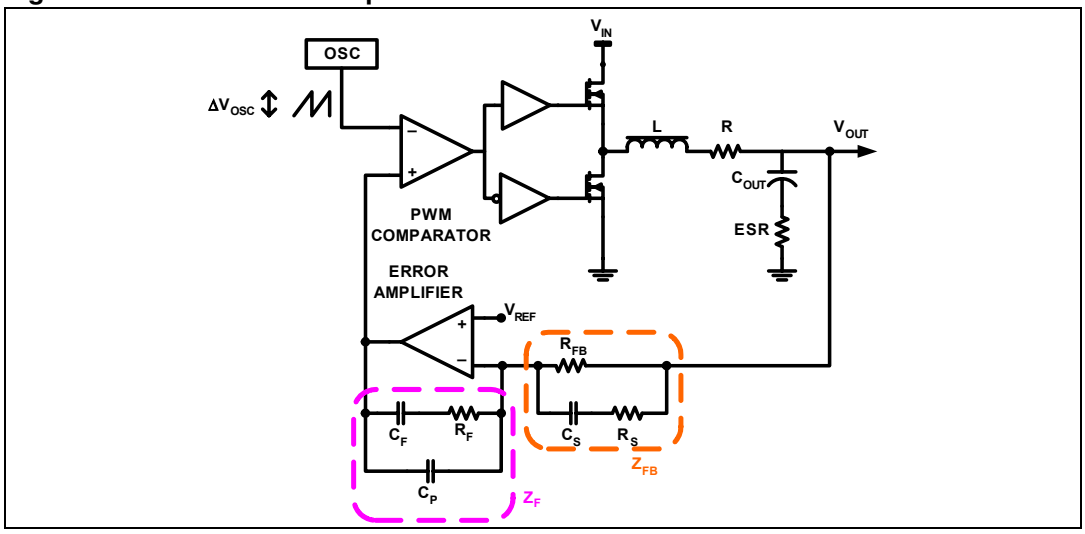
The control loop showed in *Figure 6* is a voltage mode control loop. The error amplifier is a voltage mode type. The output voltage is regulated to the internal reference (when present, offset resistor between FB node and GND can be neglected in control loop calculation).

Error Amplifier output is compared to oscillator saw-tooth waveform to provide PWM signal to the driver section. PWM signal is then transferred to the switching node with V_{IN} amplitude. This waveform is filtered by the output filter.

The converter transfer function is the small signal transfer function between the output of the EA and V_{OUT}. This function has a double pole at frequency F_{LC} depending on the L-C_{OUT} resonance and a zero at F_{ESR} depending on the output capacitor ESR. The DC Gain of the modulator is simply the input voltage V_{IN} divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

The compensation network closes the loop joining V_{OUT} and EA output with transfer function ideally equal to $-Z_F / Z_{FB}$.

Figure 6. PWM control loop

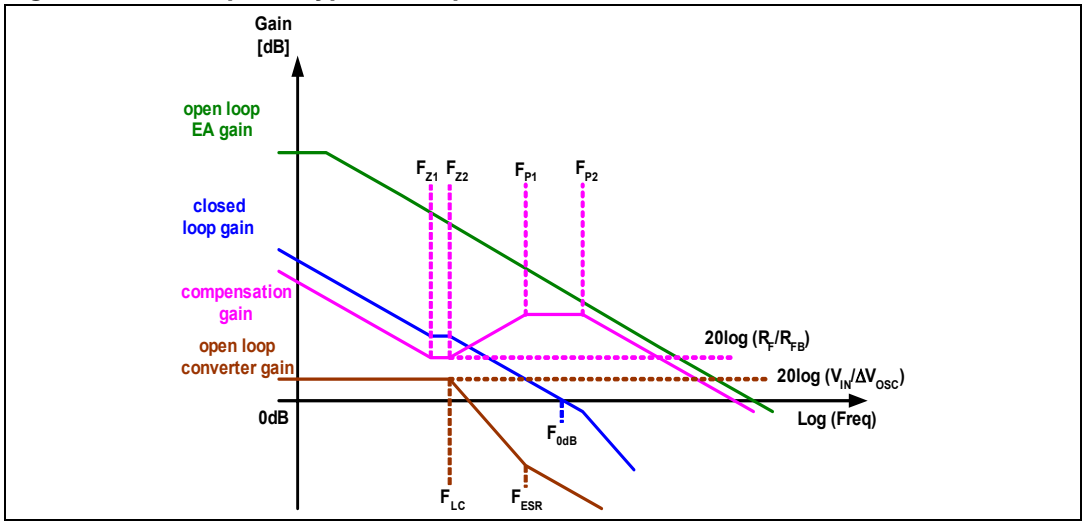


Compensation goal is to close the control loop assuring high DC regulation accuracy, good dynamic performances and stability. To achieve this, the overall loop needs high DC gain, high bandwidth and good phase margin.

High DC gain is achieved giving an integrator shape to compensation network transfer function. Loop bandwidth (F_{0dB}) can be fixed choosing the right R_F/R_{FB} ratio, however, for stability, it should not exceed $F_{SW}/2\pi$. To achieve a good phase margin, the control loop gain has to cross 0dB axis with -20dB/decade slope.

As an example, *Figure 7* shows an asymptotic bode plot of a type III compensation.

Figure 7. Example of type III compensation.



- Open loop converter singularities:

a) $$F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}}$$

b) $$F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot ESR}$$

- Compensation Network singularities frequencies:

a) $$F_{Z1} = \frac{1}{2\pi \cdot R_F \cdot C_F}$$

b) $$F_{Z2} = \frac{1}{2\pi \cdot (R_{FB} + R_S) \cdot C_S}$$

c) $$F_{P1} = \frac{1}{2\pi \cdot R_F \cdot \left(\frac{C_F \cdot C_P}{C_F + C_P}\right)}$$

d) $$F_{P2} = \frac{1}{2\pi \cdot R_S \cdot C_S}$$

To place the poles and zeroes of the compensation network, the following suggestions may be followed:

a) Set the gain R_F/R_{FB} in order to obtain the desired closed loop regulator bandwidth according to the approximated formula (suggested values for R_{FB} range from 2kΩ to 5kΩ):

$$\frac{R_F}{R_{FB}} = \frac{F_{0dB}}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN}}$$

b) Place F_{Z1} below F_{LC} (typically 0.5*F_{LC}):

$$C_F = \frac{1}{\pi \cdot R_F \cdot F_{LC}}$$

c) Place F_{P1} at F_{ESR}:

$$C_P = \frac{C_F}{2\pi \cdot R_F \cdot C_F \cdot F_{ESR} - 1}$$

d) Place F_{Z2} at F_{LC} and F_{P2} at half of the switching frequency:

$$R_S = \frac{R_{FB}}{\frac{F_{SW}}{2 \cdot F_{LC}} - 1}$$

$$C_S = \frac{1}{\pi \cdot R_S \cdot F_{SW}}$$

e) Check that compensation network gain is lower than open loop EA gain;

f) Estimate phase margin obtained (it should be greater than 45°) and repeat, modifying parameters, if necessary.

9.3 Layout guidelines

L6727 provides control functions and high current integrated drivers to implement high-current step-down DC-DC converters. In this kind of application, a good layout is very important.

The first priority when placing components for these applications has to be reserved to the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (EMI and losses) power connections (highlighted in *Figure 8*) must be part of a power plane and anyway realized by wide and thick copper traces: loop must be anyway minimized. The critical components, i.e. the power MOSFETs, must be close one to the other. The use of multi-layer printed circuit board is recommended.

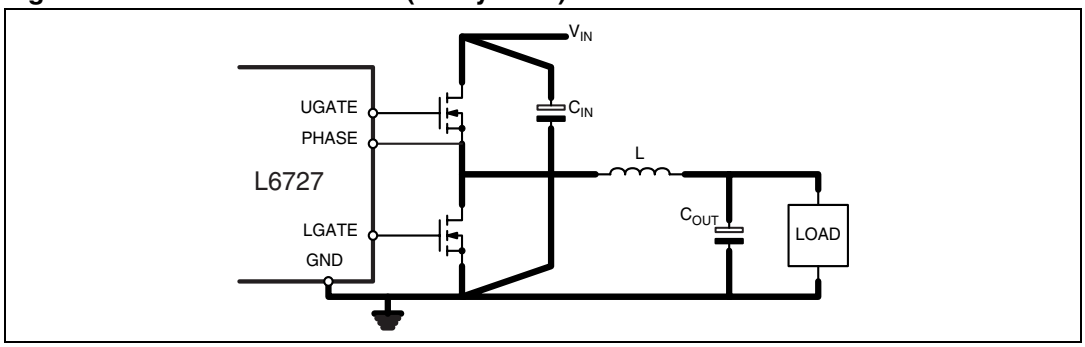
The input capacitance (C_{IN}), or at least a portion of the total capacitance needed, has to be placed close to the power section in order to eliminate the stray inductance generated by the copper traces. Low ESR and ESL capacitors are preferred, MLCC are suggested to be connected near the HS drain.

Use proper VIAs number when power traces have to move between different planes on the PCB in order to reduce both parasitic resistance and inductance. Moreover, reproducing the

same high-current trace on more than one PCB layer will reduce the parasitic resistance associated to that connection.

Connect output bulk capacitors (C_{OUT}) as near as possible to the load, minimizing parasitic inductance and resistance associated to the copper trace, also adding extra decoupling capacitors along the way to the load when this results in being far from the bulk capacitors bank.

Figure 8. Power connections (heavy lines)

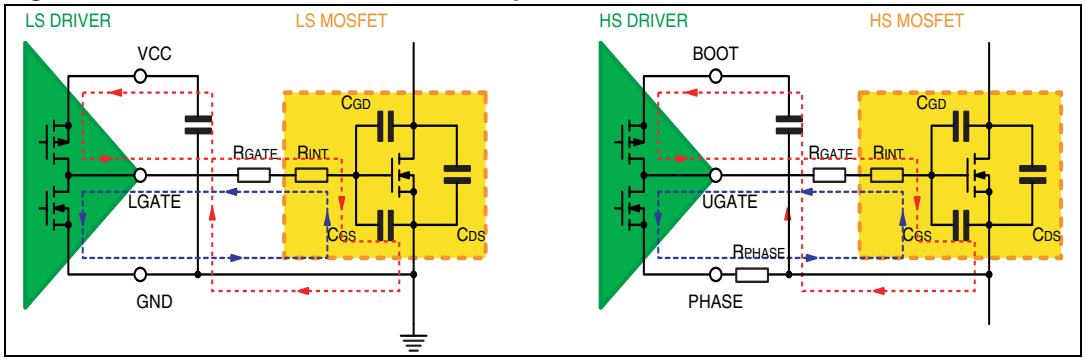


Gate traces and phase trace must be sized according to the driver RMS current delivered to the power MOSFET. The device robustness allows managing applications with the power section far from the controller without losing performances. Anyway, when possible, it is recommended to minimize the distance between controller and power section. See *Figure 9* for drivers current paths.

Small signal components and connections to critical nodes of the application, as well as bypass capacitors for the device supply, are also important. Locate bypass capacitor (VCC and Bootstrap capacitor) and loop compensation components as close to the device as practical. For over current programmability, place R_{OCSET} close to the device and avoid leakage current paths on COMP / OC pin, since the internal current source is only 60µA.

Systems that do not use Schottky diode in parallel to the Low-Side MOSFET might show big negative spikes on the phase pin. This spike must be limited within the absolute maximum ratings (for example, adding a gate resistor in series to HS MOSFET gate, or a phase resistor in series to PHASE pin), as well as the positive spike, but has an additional consequence: it causes the bootstrap capacitor to be over-charged. This extra-charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage overcomes the absolute maximum ratings also causing device failures. It is then suggested in this cases to limit this extra-charge by adding a small resistor in series to the bootstrap diode (R_D in *Figure 1*).

Figure 9. Drivers turn-on and turn-off paths



9.4 Embedding L6727-based VRs

When embedding the VR into the application, additional care must be taken since the whole VR is a switching DC/DC regulator and the most common system in which it has to work is a digital system such as MB or similar. In fact, latest MBs have become faster and more powerful: high speed data busses are more and more common and switching-induced noise produced by the VR can affect data integrity if additional layout guidelines are not followed. Few easy points must be considered mainly when routing traces in which switching high currents flow (switching high currents cause voltage spikes across the stray inductance of the traces causing noise that can affect the near traces):

When reproducing high current path on internal layers, keep all layers the same size in order to avoid "surrounding" effects that increase noise coupling.

Keep safe guard distance between high current switching VR traces and data busses, especially if high-speed data busses, to minimize noise coupling.

Keep safe guard distance or filter properly when routing bias traces for I/O sub-systems that must walk near the VR.

Possible causes of noise can be located in the PHASE connections, MOSFETs gate drive and Input voltage path (from input bulk capacitors and HS drain). Also GND connection must be considered if not insisting on a power ground plane. These connections must be carefully kept far away from noise-sensitive data busses.

Since the generated noise is mainly due to the switching activity of the VR, noise emissions depend on how fast the current switches. To reduce noise emission levels, it is also possible, in addition to the previous guidelines, to reduce the current slope and thus to increase the switching times: this will cause, as a consequence of the higher switching time, an increase in switching losses that must be considered in the thermal design of the system.

10 Package mechanical data

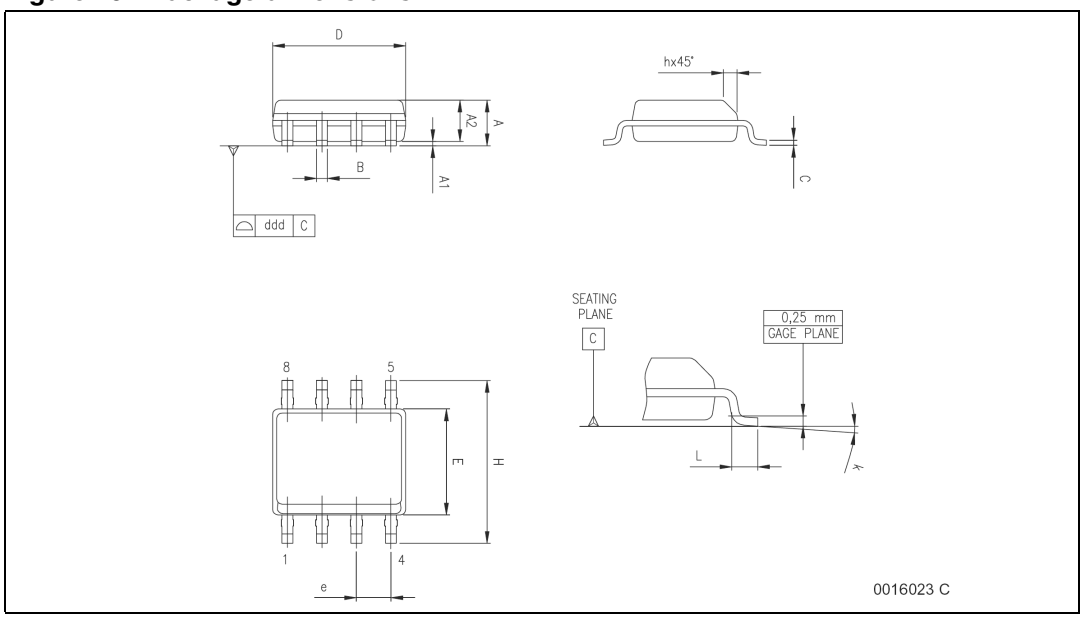
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 6. SO-8 Mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. D and F does not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch) per side.

Figure 10. Package dimensions



11 Revision history

Table 7. Revision history

Date	Revision	Changes
04-Dec-2006	1	Initial release.
28-Feb-2007	2	Updated V_{OCTH} values in *Table 5 on page 7*
06-Jun-2007	3	Updated *Figure 1: Typical application circuit on page 4*, *Table 3* and *Table 4 on page 6*